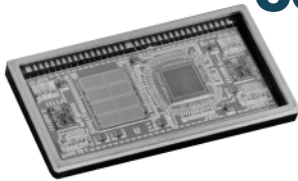


SPACE LEVEL MIL-STD-1553 BC/RT/MT ADVANCED COMMUNICATION ENGINE (SP'ACE) TERMINAL



ACE User's Guide
Also Available



DESCRIPTION

DDC's BU-61582 Space Advanced Communication Engine (SP'ACE) is a radiation hardened version of the BU-61580 ACE terminal. DDC is able to supply the BU-61582 with enhanced screening for space and other high reliability applications.

The BU-61582 provides a complete integrated BC/RT/MT interface between a host processor and a MIL-STD-1553 bus. The BU-61582 provides functional and software compatibility with the standard BU-61580 product and is packaged in the same 1.9-square-inch package footprint.

As an option, DDC can supply the BU-61582 with space level screening. This entails enhancements in the

areas of element evaluation and screening procedures for active and passive elements, as well as the manufacturing and screening processes used in producing the terminals.

The BU-61582 integrates dual transceiver, protocol, memory management and processor interface logic, and 16K words of RAM in the choice of 70-pin DIP or flat pack packages. Transceiverless versions may be used with an external electrical or fiber optic transceiver.

To minimize board space and 'glue' logic, the SP'ACE terminals provide ultimate flexibility in interfacing to a host processor and internal/external RAM.

FEATURES

- **Radiation-Hardened to 1 MRad**
- **Fully Integrated 1553 Terminal**
- **Flexible Processor Interface**
- **16K x 16 Internal RAM**
- **Automatic BC Retries**
- **Programmable BC Gap Times**
- **BC Frame Auto-Repeat**
- **Intelligent RT Data Buffering**
- **Small Ceramic Package**
- **Available to SMD 5962-96887**

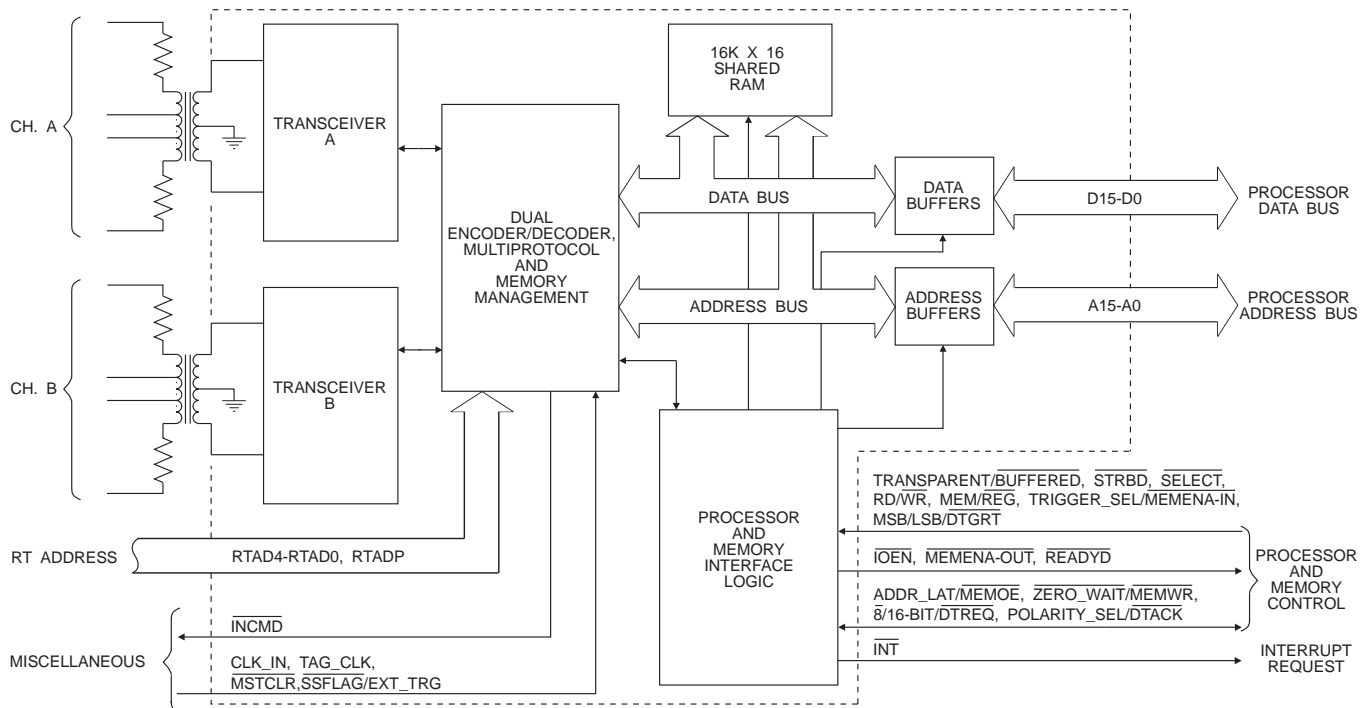
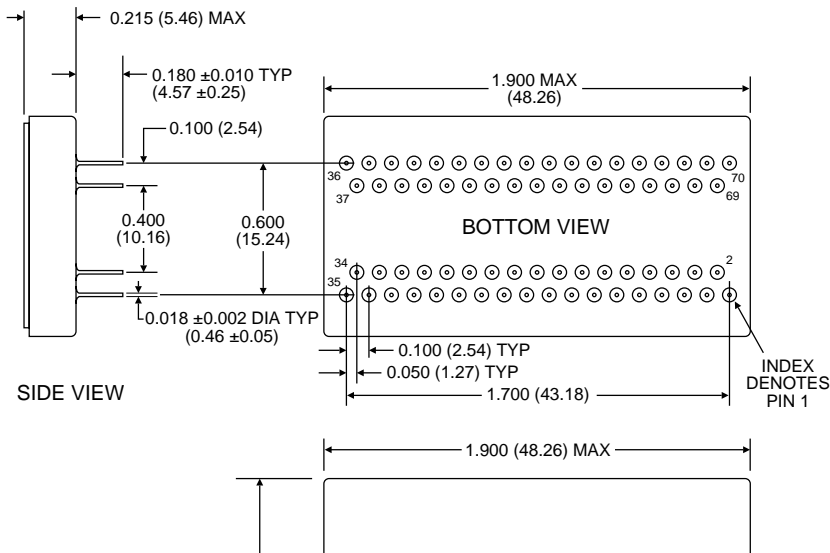


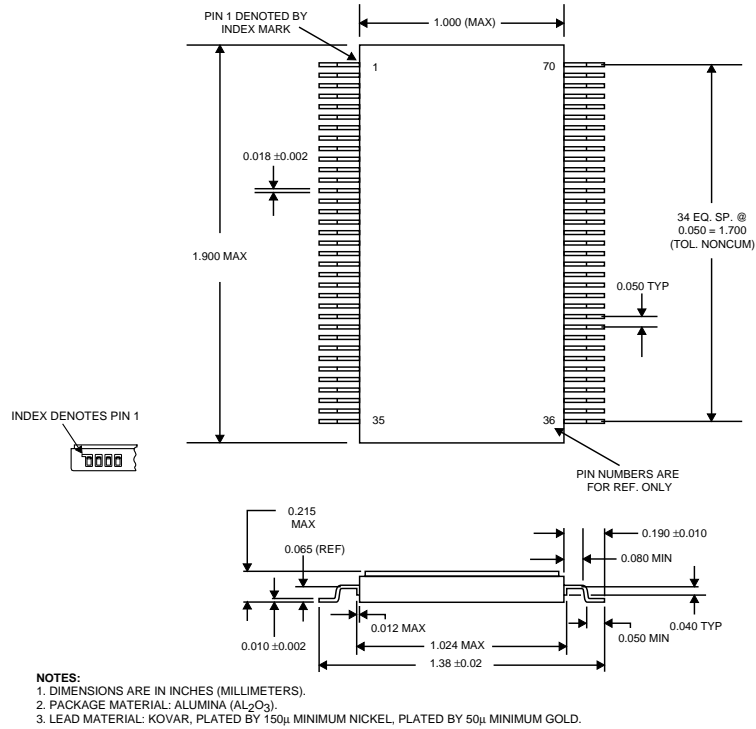
FIGURE 1. BU-61582 BLOCK DIAGRAM

SP'ACE SERIES RADIATION SPECIFICATIONS			
PART NUMBER	TOTAL DOSE	SINGLE EVENT UPSET	SINGLE EVENT LATCHUP
BU-61582XX	1MRad	3.6 x 10 ⁻⁵ errors/device-day, (LET Threshold of 59 MeV/mg/cm ²)	Immune

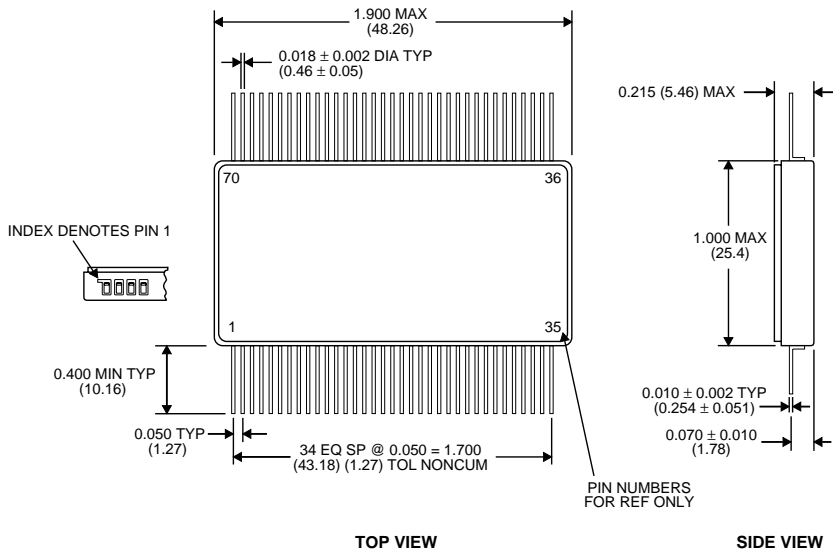
HIGH RELIABILITY SCREENING OPTIONS	
ELEMENT EVALUATION	METHOD
Visual Inspection: Integrated Circuits Transistors & Diodes Passive Components	MIL-STD-883, Method 2010 Condition A MIL-STD-750, Method 2072 and 2073 MIL-STD-883, Method 2032 Class S
SEM Analysis for Integrated Circuits	MIL-STD-883, Method 2018
Element Evaluation: Visual, Electrical, Wire Bondability, 24-Hour Stabilization Bake, 10 Temperature Cycles 5000 g's constant acceleration 240-Hour Powered Burn-In and 1000-Hour Life Test (Burn-In and 1000-Hour Life Test Are Only Required For Active Components.)	MIL-H-38534
ASSEMBLY & TEST	
Particle Impact Noise Detection (PND)	MIL-STD-883, Method 2020 Condition A
320-Hour Burn-In	MIL-STD-883, Method 1015
100% Non-Destructive Wirebond Pull	MIL-STD-883, Method 2023
Radiographic (X-Ray) Analysis	MIL-STD-883, Method 2012
QCI TESTING	
Extended Temperature Cycling: 20 Cycles Including Radiographic (X-Ray) Testing	MIL-STD-883, Method 1010 Condition C and MIL-STD-883, Method 2012
Moisture Content Limit of 5000 PPM	MIL-STD-883, Method 1018



BU-61582DX, 70-PIN DIP CERAMIC PACKAGE MECHANICAL OUTLINE



BU-61582GX, 70-PIN GULL LEAD CERAMIC PACKAGE MECHANICAL OUTLINE



- NOTES:**
 1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
 2. PACKAGE MATERIAL: ALUMINA (AL₂O₃).
 3. LEAD MATERIAL: KOVAR, PLATED BY 150μ MINIMUM NICKEL, PLATED BY 50μ MINIMUM GOLD.

BU-61582FX, 70-PIN FLAT PACK CERAMIC PACKAGE MECHANICAL OUTLINE

ORDERING INFORMATION

BU-61582XX-XXXX

Supplemental Process Requirements:

- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Other Criteria:

- 0 = No X Ray
- 1 = X Ray

Process Requirements:

- 0 = Standard DDC Processing, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant*
- 2 = B**
- 3 = MIL-PRF-38534 Compliant with PIND Testing*
- 4 = MIL-PRF-38534 Compliant with Solder Dip*
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip*
- 6 = B** with PIND Testing
- 7 = B** with Solder Dip
- 8 = B** with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See page xiii.)

Temperature Grade/Data Requirements:

- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Voltage Transceiver Option:

- 0 = No Transceiver
- 1 = +5/-15 V
- 2 = +5/-12 V

Package:

- D = DIP
- F = Flat Pack
- G = Gull Leads (Above "Process Requirements" must include solder dip.)

Product Type:

- 61582 = 70-Pin BC/RT/MT with 16K x 16 Internal RAM
- 61583 = 70-Pin BC/RT/MT with 16K x 16 Internal RAM and with RT Address Latch

*MIL-PRF-38534 Compliant products include 320 hours of burn-in and 100% non-destruct pull-test. "Supplemental Process Requirements" must be an "L" or a "Q" for MIL-PRF-38534 compliant parts.

**Standard DDC Processing with burn-in and full temperature test.

NOTES

NOTES

NOTES

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.



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